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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/631,726	SINHAROY, BALARAM	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2000 and 18 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-20 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 18 December 2000.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The disclosure is objected to because of the following informalities: Please put in the serial number of Attorney Docket No. AUS9-2000-0481-US1 on page 1. Appropriate correction is required.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Horton et al., U.S. Patent Number 6,223,280 (herein referred to as Horton) in view of Rahman et al., U.S. Patent Number 5,805,878 (herein referred to as Rahman).

8. Referring to claim 1, Horton has taught a method of generating a global history vector comprising the steps of:

a. Determining if a branch instruction is present (Horton column 8, lines 34-49 and Figure 4).

b. Maintaining a current global history vector in a shift register when the selected group does not contain a branch instruction (Horton column 8, lines 34-55 and Figure 4). In regards to Horton, the branch prediction elements are changed when a branch is detected.

c. Shifting a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is predicted as a branch taken (Horton Abstract; column 2, line 43 to column 3, line 14; column 8, line 63 to column 9, line 16; Figure 2; Figure 3; and Figure 4).

d. Shifting a second value into the shift register to generate a second vector when the selected group contains a branch instruction and the selected group does not include a branch instruction predicted as a branch taken (Horton Abstract; column 2, line 43 to column 3, line 14; column 8, line 63 to column 9, line 16; Figure 2; Figure 3; and Figure 4).

9. Horton has not explicitly taught fetching a selected group of instructions. However, Horton has taught fetching instructions to and from an instruction cache (Horton column 4, lines 66-67 and Figure 1). Rahman has taught fetching a selected group of instructions (Rahman column 4, lines 42-61). A person of ordinary skill in the art at the time the invention was made, and as taught by Rahman, would have recognized that fetching a group of instructions from an

instruction cache improves performance of the processor (Rahman column 4, lines 47-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the selected group of instructions of Rahman in the device of Horton to improve processor performance.

10. Referring to claim 2, Horton has taught the step of storing the generated value in an entry in a branch instruction queue associated with the selected group of instructions (Horton Abstract; column 2, line 43 to column 3, line 14; column 9, line 66 to column 10, line 2; Figure 2; Figure 3; and Figure 4).

11. Referring to claim 3, Horton has taught the step of correcting the generated vector upon a misprediction (Horton column 2, lines 29-32 and column 9, lines 20-23) comprising the substeps of:

a. Retrieving a selected number of bits of the vector stored from the branch instruction queue into the shift register (Horton column 9, lines 20-65 and Figure 4); and

b. Shifting an updated history bit into the shift register (column 9, lines 20-65 and Figure 4).

12. Referring to claim 4, Horton has taught wherein the first value comprises a logic 1 and the second value is a logic 0 (Horton column 2, line 66 to column 3, line 1).

13. Referring to claim 5, Horton has not explicitly taught wherein the selected group of instructions comprises eight instructions. However, Horton has taught fetching instructions to and from an instruction cache (Horton column 4, lines 66-67 and Figure 1). Rahman has taught wherein the selected group of instructions comprises eight instructions (Rahman column 4, lines

42-61). In regards to Rahman, one or more instructions are fetched, which includes eight instructions fetched. (Rahman column 4, lines 42-61). A person of ordinary skill in the art at the time the invention was made, and as taught by Rahman, would have recognized that fetching a group of instructions to and from an instruction cache improves performance of the processor (Rahman column 4, lines 47-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the selected group of instructions of Rahman in the device of Horton to improve processor performance.

14. Referring to claim 6, Horton has taught a method of performing branch predictions comprising the steps of:

a. Indexing a branch history table using a first global history vector to retrieve a first prediction value (Horton column 2, line 43 to column 3, line 14);

b. Generating a second global history vector (Rahman column 4, lines 42-61) comprising the substeps of:

i. Retaining the first vector when at least one branch instruction is not present (Horton column 8, lines 34-55 and Figure 4);

ii. Appending a bit of a first value to the first vector at least one branch instruction is predicted to be a branch taken (Horton Abstract; column 2, line 43 to column 3, line 14; column 8, line 63 to column 9, line 16; Figure 2; Figure 3; and Figure 4); and

iii. Appending a bit of a second value to the first vector when at least one branch instruction is present and contains no branch instructions predicted to be a branch taken (Horton Abstract; column 2, line 43 to column 3, line

14; column 8, line 63 to column 9, line 16; Figure 2; Figure 3; and Figure 4); and

c. Indexing the branch history table using the second global history vector during a second fetch cycle to retrieve a second branch prediction value (Horton Abstract; column 2, line 43 to column 3, line 14; column 9, line 66 to column 10, line 20; Figure 2; Figure 3; and Figure 4).

15. Horton has not explicitly taught fetching a selected group of instructions. However, Horton has taught fetching instructions to and from an instruction cache (Horton column 4, lines 66-67 and Figure 1). Rahman has taught fetching a selected group of instructions (Rahman column 4, lines 42-61). A person of ordinary skill in the art at the time the invention was made, and as taught by Rahman, would have recognized that fetching a group of instructions to and from an instruction cache improves performance of the processor (Rahman column 4, lines 47-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the selected group of instructions of Rahman in the device of Horton to improve processor performance.

16. Referring to claim 7, Horton has taught the step of storing the first and second vectors in an entry of a branch history queue associated with the first branch (Horton Abstract; column 2, line 43 to column 3, line 14; column 9, line 66 to column 10, line 20; Figure 2; Figure 3; and Figure 4). Horton has not explicitly taught fetching a selected group of instructions. However, Horton has taught fetching instructions to and from an instruction cache (Horton column 4, lines 66-67 and Figure 1). Rahman has taught fetching a selected group of instructions (Rahman column 4, lines 42-61). A person of ordinary skill in the art at the time the invention was made,

and as taught by Rahman, would have recognized that fetching a group of instructions from an instruction cache improves performance of the processor (Rahman column 4, lines 47-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the selected group of instructions of Rahman in the device of Horton to improve processor performance.

17. Referring to claim 8, Horton has taught:

a. Detecting a branch misprediction based on the first prediction value (Horton column 2, lines 29-32 and column 9, lines 20-23);

b. Retrieving the first and second vectors from the branch history queue (Horton column 2, line 43 to column 3, line 14; column 9, line 66 to column 10, line 20; Figure 2; Figure 3; and Figure 4);

c. Indexing the branch history table using the first vector to correct the first prediction value (Horton Abstract; column 2, line 43 to column 3, lines 14; column 9, line 20 to column 10, line 20; Figure 2; Figure 3; and Figure 4); and

d. Appending a corrected bit to the second vector to generate a corrected branch history vector (Horton column 9, lines 20-6 and Figure 4).

18. Referring to claim 9, Horton has taught wherein said first fetch cycle precedes the second fetch cycle by three fetch cycles (Horton column 1, line 49 to column 2, line 32). In regards to Horton, he has taught that the instruction pipeline requires a certain number of cycles before another instruction is fetched for the pipeline.

19. Referring to claim 10, Horton has taught wherein said steps of indexing comprises the step of gating the vector with selected bits of a current instruction address (Horton column 10, lines 13-18).

20. Referring to claim 11, Horton has taught wherein said steps of gating comprise the steps of performing XOR operations (Horton column 10, lines 13-18).

21. Referring to claim 12, Horton has taught wherein said substeps of appending comprise the substeps of shifting a bit into a shift register storing the first vector (Horton Abstract; column 2, line 43 to column 3, line 14; column 8, line 63 to column 9, line 16; column 9, lines 20-65; Figure 2; Figure 3; and Figure 4).

22. Referring to claim 13, Horton has taught branch processing circuitry comprising:

a. A shift register for storing a global history vector (Horton Abstract; column 8, line 63 to column 9, line 2; and Figure 2);

b. Control circuitry for selectively updating a first global history vector stored in said shift register (Horton column 8, lines 34-67 and Figure 2) operable to:

i. Determine a branch instruction is present (Horton column 8, lines 34-49 and Figure 4);

ii. Maintain said first global history vector in said shift register when the selected group does not contain a branch instruction (Horton column 8, lines 34-55 and Figure 4). In regards to Horton, the branch prediction elements are changed when a branch is detected.

iii. Shift a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is

predicted as a branch taken (Horton Abstract; column 2, line 43 to column 3, line 14; column 8, line 63 to column 9, line 16; Figure 2; Figure 3; and Figure 4); and

iv. Shifting a second value into the shift register to generate a second vector when the selected group contains a branch instruction and does not contain a branch instruction predicted as a branch taken (Horton Abstract; column 2, line 43 to column 3, line 14; column 8, line 63 to column 9, line 16; Figure 2; Figure 3; and Figure 4).

23. Horton has not explicitly taught fetching a selected group of instructions. However, Horton has taught fetching instructions to and from an instruction cache (Horton column 4, lines 66-67 and Figure 1). Rahman has taught fetching a selected group of instructions (Rahman column 4, lines 42-61). A person of ordinary skill in the art at the time the invention was made, and as taught by Rahman, would have recognized that fetching a group of instructions to and from an instruction cache improves performance of the processor (Rahman column 4, lines 47-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the selected group of instructions of Rahman in the device of Horton to improve processor performance.

24. Referring to claim 14, Horton has taught a branch history table (Horton Abstract; column 8, line 63 to column 9, line 2; and Figure 2) and circuitry for generating an index to an entry in said branch history table using selected bits from a current address and selected bits of said first vector to retrieve a prediction value stored therein (Horton Abstract; column 2, line 43 to column 3, line 14; column 9, line 66 to column 10, line 20; Figure 2; Figure 3; and Figure 4).

25. Referring to claim 15, Horton has taught circuitry for updating said second vector when said prediction value results in a misprediction (Horton column 2, line 29-32 and column 9, lines 20-23) comprising:

a. A queue for storing said first and said second vectors (Horton Abstract; column 8, line 63 to column 9, line 2; column 9, lines 20-65; Figure 2; and Figure 4). In regard to Horton, the registers act like the queue, they store the vectors.

b. Circuitry for accessing said vectors from said queue (Horton column 9, lines 20-65 and Figure 4);

c. Circuitry for indexing said branch history table with said first vector and updating a corresponding entry with a corrected prediction value (Horton column 9, lines 20-65 and Figure 4); and

d. Circuitry for updating a vector in said shift register with said second vector (Horton column 9, lines 20-65 and Figure 4); and

e. Circuitry for shifting the corrected prediction value into said shift register (Horton column 9, lines 20-65 and Figure 4).

26. Referring to claim 16, Horton has taught wherein said branch processing circuitry forms a portion of a single-chip microprocessor (Horton column 4, lines 47-59 and Figure 1).

27. Referring to claim 17, Horton has taught a processing system comprising:

a. A microprocessor (Horton column 4, lines 47-59 and Figure 1) comprising:

i. A branch history table for storing branch prediction values (Horton Abstract; column 8, line 63 to column 9, line 2; and Figure 2);

ii. A global history shift register for storing a global branch history vector (Horton Abstract; column 8, line 63 to column 9, line 2; and Figure 2);

iii. Logic for generating an index to said branch history table and accessing prediction values stored therein using selected bits of a said branch history vector stored in said shift register (Horton Abstract; column 2, line 43 to column 3, line 14; column 9, line 66 to column 10, line 20; Figure 2; Figure 3; and Figure 4); and

iv. Control circuitry for updating a said global branch history vector stored in said shift register (Horton column 8, lines 34-67 and Figure 2) and operable to:

(1) Retain a current vector stored in said shift register when at least one branch instruction is not present (Horton column 8, lines 34-55 and Figure 4);

(2) Shift a bit of a first value into said shift register to generate an updated vector when the selected fetch group has at least one branch instruction predicted to be a branch taken (Horton Abstract; column 2, line 43 to column 3, line 14; column 9, line 63 to column 9, line 16; Figure 2; Figure 3; and Figure 4); and

(3) Shift a bit of a second value into said shift register when said selected fetch group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken

(Horton Abstract; column 2, line 43 to column 3, line 14; column 9, line 63 to column 9, line 16; Figure 2; Figure 3; and Figure 4).

28. Horton has not explicitly taught fetching a selected group of instructions. However, Horton has taught fetching instructions to and from an instruction cache (Horton column 4, lines 66-67 and Figure 1). Rahman has taught fetching a selected group of instructions (Rahman column 4, lines 42-61). A person of ordinary skill in the art at the time the invention was made, and as taught by Rahman, would have recognized that fetching a group of instructions to and from an instruction cache improves performance of the processor (Rahman column 4, lines 47-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the selected group of instructions of Rahman in the device of Horton to improve processor performance.

29. Referring to claim 18, Horton has taught wherein said microprocessor further comprises:

a. A branch instruction queue having a plurality of entries for storing at least first and second corresponding global history vectors (Horton Abstract; column 8, line 63 to column 9, line 2; and Figure 2);

b. Circuitry for detecting a misprediction associated with a said prediction value retrieved from said branch history table and corresponding to said first global history vector in said branch instruction queue (Horton column 2, lines 29-32; column 9, lines 20-65; Figure 2; and Figure 4);

c. Circuitry for retrieving said first vector from said branch instruction queue and accessing a corresponding entry in said branch history table to correct said prediction value stored therein (Horton column 9, lines 20-65 and Figure 4); and

d. Circuitry for retrieving and modifying said second vector to generate a corrected vector in said shift register (Horton column 9, lines 20-65 and Figure 4).

30. Horton has not explicitly taught fetching a selected group of instructions. However, Horton has taught fetching instructions to and from an instruction cache (Horton column 4, lines 66-67 and Figure 1). Rahman has taught fetching a selected group of instructions (Rahman column 4, lines 42-61). A person of ordinary skill in the art at the time the invention was made, and as taught by Rahman, would have recognized that fetching a group of instructions to and from an instruction cache improves performance of the processor (Rahman column 4, lines 47-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the selected group of instructions of Rahman in the device of Horton to improve processor performance.

31. Referring to claim 19, Horton has taught wherein said processing system further includes a system memory coupled to said microprocessor (Horton column 4, lines 60-63 and Figure 1). Horton has not taught a system memory coupled to said microprocessor by a bus. Rahman has taught a system memory coupled to said microprocessor by a bus (Rahman column 7, lines 54-60 and Figure 2). A person of ordinary skill in the art at the time the invention was made, and as taught by Rahman, would recognize that a bus communicates information between the memory and microprocessor (Rahman column 7, line 55). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the bus of Rahman in the device of Horton to communicate between the memory and microprocessor.

32. Referring to claim 20, Horton has not explicitly taught wherein the selected group of instructions comprises eight instructions. However, Horton has taught fetching instructions to

and from an instruction cache (Horton column 4, lines 66-67 and Figure 1). Rahman has taught wherein the selected group of instructions comprises eight instructions (Rahman column 4, lines 42-61). In regards to Rahman, one or more instructions are fetched, which includes eight instructions fetched. (Rahman column 4, lines 42-61). A person of ordinary skill in the art at the time the invention was made, and as taught by Rahman, would have recognized that fetching a group of instructions to and from an instruction cache improves performance of the processor (Rahman column 4, lines 47-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the selected group of instructions of Rahman in the device of Horton to improve processor performance.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Pan et al., U.S. Patent Number 5,553,253, has taught branch prediction with a branch history shift register.

b. Talcott et al., U.S. Patent Number 5,857,098, has taught branch prediction with a branch history shift register.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

36. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

August 24, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100